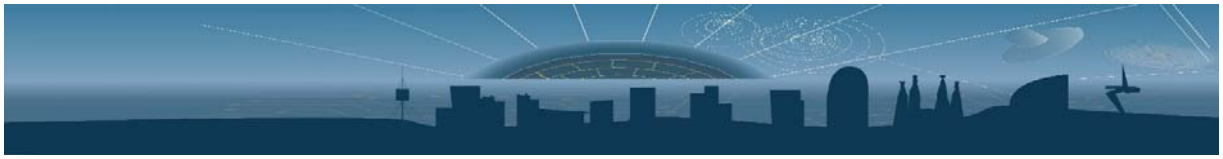

HRFLEXTOT

High Resolution Flexible Time over Threshold ASIC

User Manual

Issue:	Subject to changes
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Table of contents

List of Figures

List of Tables

1 HRFlexToT PCB board

This board has many IO and debug capabilities. The most important ones to test the ASIC are described herein. For more information about all the capabilities, please send an email to: support@siub.ub.edu. *Observe that all input/outputs are labelled in the PCB.*

Before performing any measurement please check the document: HRFlexToT AppNote - Measurements Procedure

1.1 HRFlexToT 16 channel testing board.

Figure 2 and Figure 1 shows an example of 16 channel demonstrator board to test the HRFlexToT ASIC.

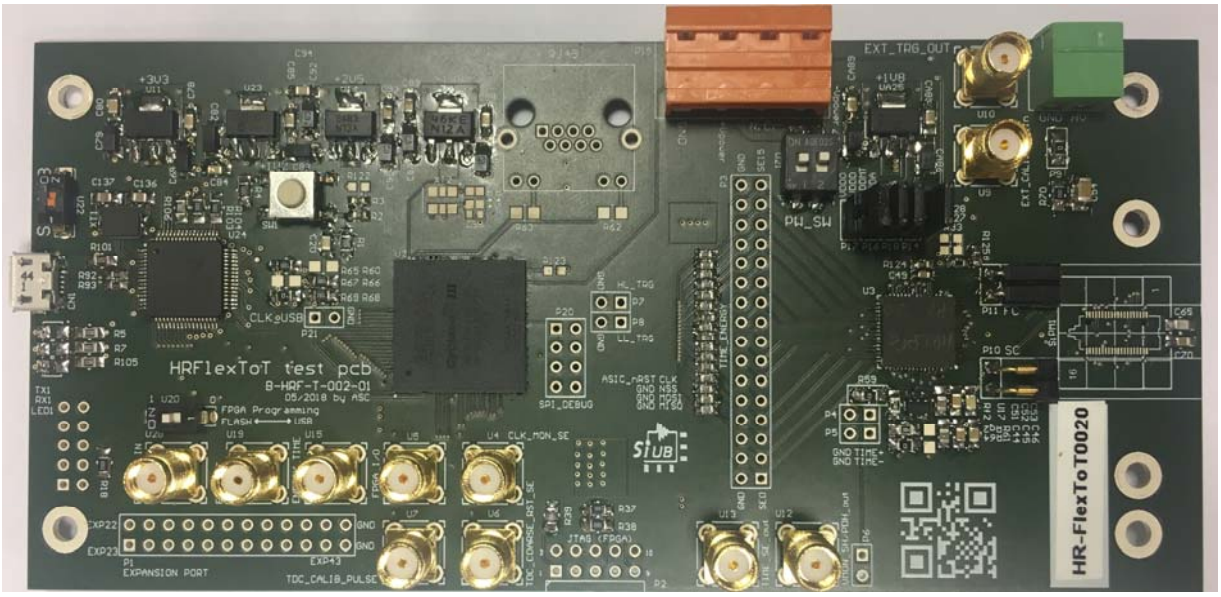


Figure 2: Top side of the HRFlexToT board.

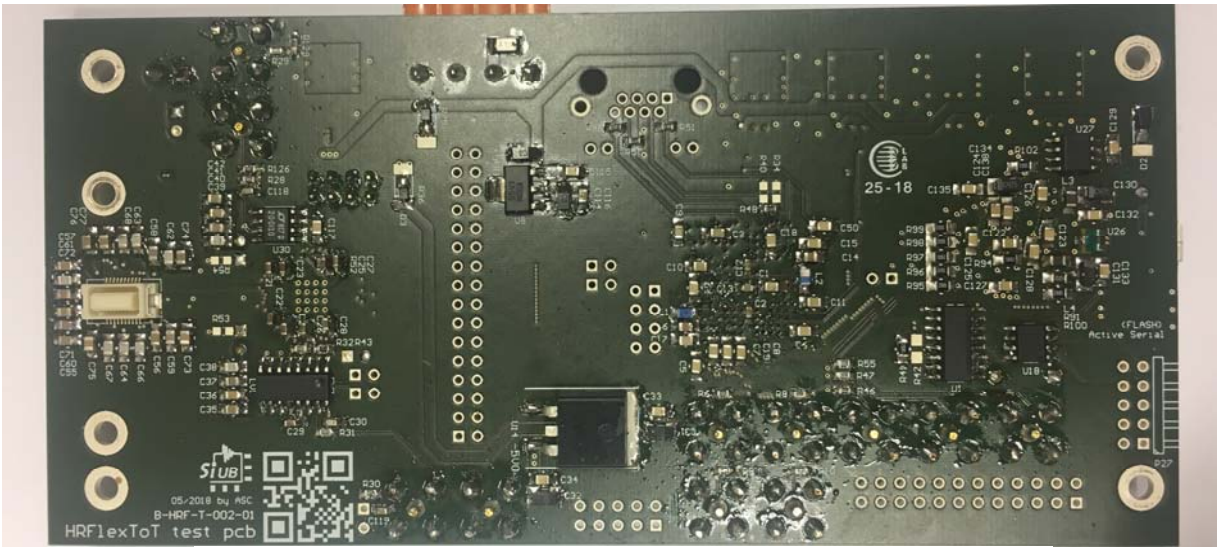


Figure 1: Bottom side of HRFlexToT board.

1.2 HRFlexToT power supply connectors.

The low voltage (LV) power supply pins are:

Pin	Signal
1	GND
2	Vpower: 6.5 Volts
3	Not Connected (NC)
4	-Vpower: -6.5 Volts

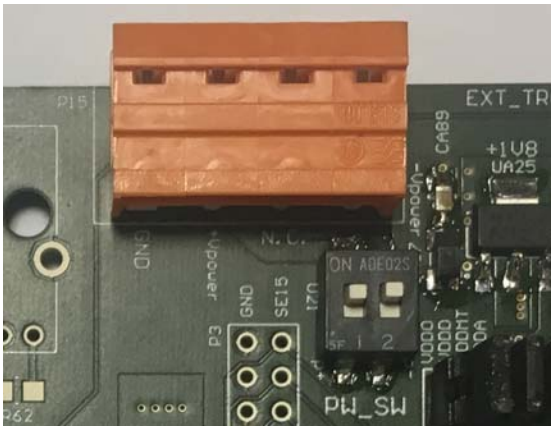


Figure 3: Low power supply connector, pin 1 corresponds to the pin located at left side.

Reference power consumption values:

Table 1: Low voltage power consumption

Instant	+Vpower	-Vpower
After reset	150-180 mA	20-40 mA.
Software running or startup	250-280 mA	20-48 mA

IMPORTANT: Limit the current of the Low Voltage power supply to a maximum of 0.4A per board to avoid damaging the PCB board.

The high voltage (HV) power supply pins are:

Pin	Signal
1	GND
2	High Voltage (HV)

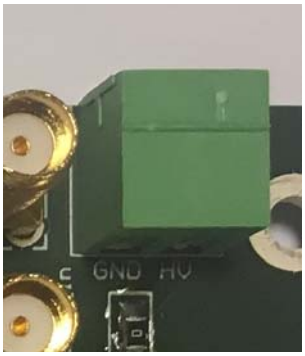


Figure 4: High power supply connector, pin 1 corresponds to the pin located at left side.

IMPORTANT: Limit the current of the High Voltage power supply to a maximum of 1mA to avoid breaking components in the PCB board.

1.3 HRFlexToT communication connectors.

USB is used to configure the board and acquire data from the 16 built-in TDCs.

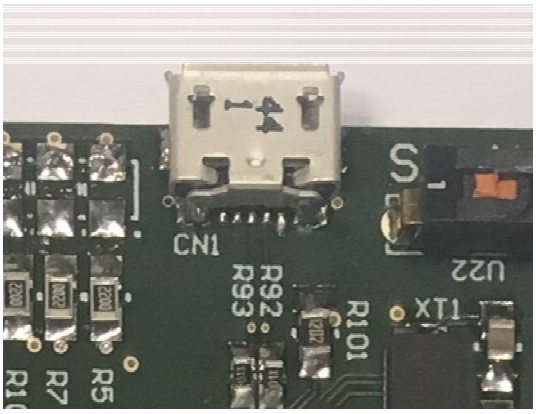


Figure 5: USB connector

1.4 HRFlexToT input/output connectors.

The demonstrator board has several input/output connectors via SMA cable to test the performance of the HRFlexToT. SMAs have a printed label in the PCB board.

1. **EXT_CALIB_VA_in (SMA U9):** This input enables the user to inject an electrical test pulse that can be used to evaluate if channels are working properly, in other words, this functionality permits to verify if signal from the input is transferred to the output as expected. This input signal must be a voltage signal; inside the ASIC is converted to current to emulate the current response of a SiPM. The software lets the user to change which is the input that will receive the test pulse (--calib_sel <N>). When the parameter is not provided, the debugging circuitry is disabled, and the input signal must come from the SiPMs' outputs. Figure 6: ·EXT_CALIB_VA_input and EXT_TRG_OUT SMA output.Figure 6 shows the location of this input in the board.
2. **EXT_TRG_OUT (SMA U10):** This output shows the trigger signal used for the energy acquisition. The different trigger options available, including an external trigger, can be configured via a software command. Figure 6 shows the location of this input in the board.

Figure 6: ·EXT_CALIB_VA_input and EXT_TRG_OUT SMA output.

3. **EXT_TRG_IN (SMA U28):** This input permits to inject a pulse to be used as a trigger signal for the energy acquisition. This trigger mode can be configured via a software command. Figure 7 shows the location of this input in the board.
4. **ENERGY_TIME (SMA U15):** this output can show the 16 HR-FlexToT Energy/Time outputs. The output to be shown is controlled via software. Figure 7 shows the location of this input in the board.

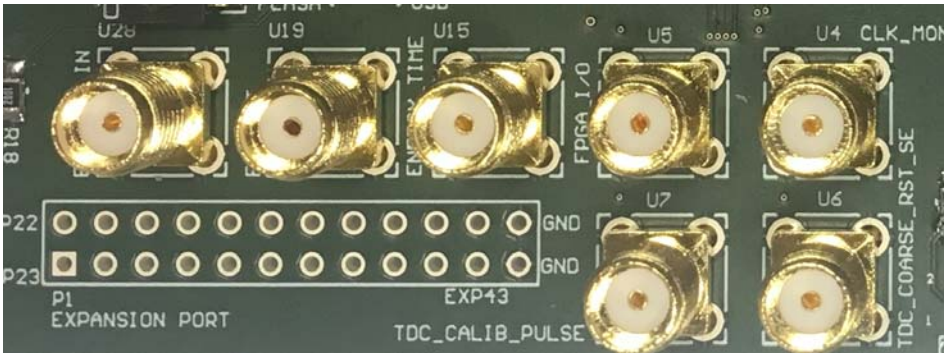


Figure 7: EXT_TRG_IN input and ENERGY_TIME SMA output.

5. **TIME_ENERGY (Socket P3):** The Time and energy can be also acquired per channel. Socket P3 enables the possibility to read these outpus per channel as shown in

Figure 8: Socket access to measure TIME/Energy per channel.

6. **VMON_SW/PDH_out:** This is the analog monitoring output which enables us to probe the internal output of the shaper and the peak detector and track and hold (PDH). Note that there is a buffer to drive the cable and an AC coupling (C119) between the ASIC and the SMA. This output is helpful to verify if the input signal is injected correctly. It is important to highlight that, the HRFlexToT board that this output comes with an AC coupling to ease the acquisition of the signal in the oscilloscope (users normally will use this output to verify the response of their sensor). If the user wants to verify the response of the peak detector, this AC coupling must be removed. Substitute Capcitor C119 (it is located near the SMA of this output in the bottom side in of the HRFlexToT board). The output to be shown is controlled via software. Figure 9 shows the location of this input in the board.
7. **TIME_SE_out:** Fast-OR timing output. This output has been converted from LVDS to 3.3 V single-ended CMOS. LVDS output is available in the test points P4 and P5. Figure 9 shows the location of this input in the board.

Figure 9: (left) TIME_SE_out and VMON_SH/PDH_out outputs; (right) location of the C119 capacito for the Accoupling of shaper/PDH signal.

2 HRFlexToT software

2.1 Installation & Drivers:

HRFlexToT is available in both Windows & Linux, and both binaries are compiled with static libraries, so no dependency problems should occur. However, it is necessary to install the FTDI drivers for the FT2232HL chip. More details and latest driver version in:

http://www.ftdichip.com/Drivers/D2XX.htm

2.2 Running the Software. Summary of commands.

HRFlexToT is command line (no GUI available). The binary contains a set of commands, each of them to perform a different task. If no extra parameters are passed, global help with the list of commands is printed:

```
$ sw/hrflextot
Usage:
 sw/hrflextot <command> <command args>*

List of available commands are:
 * version : Show current version (which is 191fcd58-2d139a57)
 * list_boards : Show connected boards
 * upload_firmware : Upload a new firmware
 * version_firmware : Show firmware version
 * tdc_calib : Calibrates built-in TDC
 * tdc_acq : Acquires data from built-in TDC
 * info : Shows HRFlexToT board useful information
 * config : Configure HRFlexTOT
 * show_config : Shows current HRFlexTOT configuration
 * threshold_scan : Performs a threshold scan
 * photon_count : Performs a Photon Count Rate (PCR) scan

For more information about a command try <command> --help
```

The list of available commands is the following:

Command	Description
hrflextot version	Shows current software version
hrflextot list_boards	Shows a list with the HR-FlexToT boards connected
hrflextot upload_firmware <args>	Allows firmware upgrade (volatile or non-volatile)
hrflextot version_firmware	Shows current firmware version
hrflextot tdc_calib <args>	Calibration of the built-in FPGA TDC.
hrflextot tdc_acq <args>	Runs TDC acquisition
hrflextot info	Shows HR-FlexToT board useful information
hrflextot config <args>	Configures HR-FlexToT electronics
hrflextot show_config [args]	Shows HR-FlexToT ASIC configuration
hrflextot threshold_scan [args]	Runs a threshold scan of the discriminators (time/trigger)
hrflextot photon_count [args]	Performs a Photon Count Rate of the 16 ASIC outputs

Table 2: HR-FlexToT software commands.

All the above-mentioned commands have the following generic options and they will be omitted in the explanation of the commands:

[-h], [--help]	Shows the command help message.
[-b], [--board]	Which board SN to use. E.g.: HR-FlexToT0018. Mandatory when multiple boards connected.
[-l], [--loglevel]	Log level (trace, debug, verbose, info, warning, error, fatal, disable).
[-F], [--logformat]	Log format ('-' to disable any header).
[-C], [--args_file]	File containing the arguments to parse. Same format as the command line flags.
Example	User has problems trying to connect with the board and wants to troubleshoot the problem. In this case, we suggest changing the default log level (info) to debug, and specify manually the serial number: hrflextot version_firmware -b HRFlexToT0018 -l debug

2.3 Detailed command description.

2.3.1 hrflextot version

Command	hrflextot version Returns the git hash corresponding to the software version. In case you need support, please, tell us which software version you are using.
Example	hrflextot version
History	Legacy command.

2.3.2 hrflextot list_boards

Command	hrflextot list_boards Shows the Serial Number (SN) of the boards connected to the PC, and the description. The SN should be unique, while the board description will be the same for the same PCB board version. E.g. B-HRF-T-002-01, corresponding to HR-FlexToT test board #1, version 2.
Example	hrflextot list_boards
History	Legacy command.

2.3.3 hrflextot upload_firmware

Command	hrflextot upload_firmware <-f *file_name*> [-d] To perform a firmware upgrade. When the *.rbf* file is used, the firmware will be available until the next board power cycle (volatile firmware). To use this capability, the switch U20 must be set to *USB*. When .rpd file is used, the firmware will be persistently stored into the Flash memory (default).

[-f] **[--file]** The path to the configuration file name to be applied.

[-d] **[--direct]** When provided, the expected firmware file is in Raw Binary Format (rbf). It will not modify the FPGA program stored into the Flash memory.

Example 1 This example programs the FPGA with a new firmware without modifying the one stored in Flash:

hrflextot upload_firmware -d -f fw/hrflextot_v1.0.rbf

History Legacy command.

2.3.4 hrflextot version_firmware

Command hrflextot version_firmware

Returns the git hash corresponding to the firmware version. In case you need support, please, tell us which firmware version you are using.

Example hrflextot version_firmware

History Legacy command.

2.3.5 hrflextot tdc_calib

Command hrflextot tdc_calib <[-e <n_evts>] [-m <n_msecs>]> <-o calib_out_file> [-D bin_dump_file] [-f n_frames] [-M rate_kevts] [-W pwidth_ns] [-p size_bytes] [-E <ch_wildcard>] [-P] [-n bin_width_ps] [-d std_ps] <-i n_stages> [-k] [-K] [-c] <-r <min_freq_mhz> <max_freq_mhz>> [-t <step_mhz>] [-s n_events]

Acquires ToT pulses for each of the 16 HR-FlexToT channel outputs and calibrates each of the TDC bins, assuming that input pulses are random and follow a uniform random distribution. If this is not possible, the calibration pulse can be used instead (SMA with the TDC_CALIB_PULSE label). When the calibration pulse is used, the 16 TDC channels will receive the same input pulse. An external Pulse Pattern Generator (PPG) is required (3.3V single-ended CMOS) to generate random pulses (> 6-ns pulse width). It is important to highlight that this procedure should only be done in case that there were evidences that TDC calibration is not valid for the current setup conditions, or after a firmware upgrade. Otherwise, please use the TDC-FPGA calibration file provided.

[-e] **[--events]** The number of total events to read before stopping acquisition. One event corresponds to a pulse, where rising edge is the Time-of-Arrival, and the difference between rising and falling edge is the pulse width.

[-m] **[--msecs]** The acquisition time of the test in milliseconds. Note that either number of events or acquisition time must be provided.

[-o] **[--calib_outfile]** The output calibration file containing the required information for the TDC-FPGA to convert acquired events into picoseconds units. The file not only contains a lookup table for each of the

sampling channels, but also information regarding the calibration conditions.

[-D] [--raw_dump_file] Dumps the data coming from the USB in raw format file. It can be useful to trace and report errors.

[-f] [--frames_between_checks] A checkpoint byte is added every N data frames coming from the USB acquisition system. This byte is useful to check data alignment and to ensure that no data is lost in the transmission. The minimum value is 16 and the maximum is 4080. The default value does not need to be changed.

[-M] [--max_rate_kevts] The maximum acquisition rate can be limited in case that the acquisition system host is not powerful enough (e.g. Raspberry Pi or similar). Apply this filter only if the number of checkpoint issues (use the -l debug option for debugging) grows substantially (hundreds of errors per second).

[-W] [--min_pwidth] This option prevents the FPGA to send TDC events the pulse of which is lower than a certain value. This is very useful to reduce the capture file size and also to prevent USB DAQ throttling. The value is specified in nanoseconds.

[-p] [--packet_size] Length (in bytes) of the USB packet to be read. Big packet sizes are more efficient in terms of throughput.

[-E] [--en_channels] This option lets the user to individually enable/disable TDC-FPGA channels. When using this option, a list of 16 values with either 0 or 1 value must be provided. Channel 0 corresponds enable corresponds to the first value, while the last value for channel 15. All channels are enabled by default.

[-P] [--calib_pulse] When this option is provided, all the TDC channels will rely on TDC_CALIB_PULSE SMA input port. This can be very useful to calibrate the board with an external pulse generator.

[-n] [--max_bin] Modifies the maximum bin width computed by the calibration software to accept the acquisition step as good. If maximum bin width is not fulfilled, TDC-FPGA sampling clock frequency will increase on the next calibration iteration until maximum frequency is reached.

[-d] [--max_std] Modifies the maximum bin width standard deviation allowed by the calibration software.

[-i] [--min_clearance] Establishes the minimum number of stages of the 64-carry chain which its delay is higher than the clock period. It is recommendable that a margin of, at least, 3 carry stages.

[-k] [--clk_mon] When this option is provided, a copy of the TDC-FPGA internal reference clock is output though TDC_CLK_MON_SE SMA output port and TDC_CLK_MON LVDS output port. This is useful to synchronize two boards with the same reference clock.

[-K] [--clk_ext] When this option is provided, TDC-FPGA will use an external reference clock.

[-c] [--coarse_rst] When this option is provided, TDC_COARSE_RST SMA port is used to reset the TDC-FPGA global coarse counter. This is useful to synchronize different boards.

[-r] [--freq_range] Mandatory. The range of TDC-FPGA internal sampling frequencies to be tested. Lower frequency values save power consumption, but makes the 64 fast-carry chains for the given clock frequency (events will be lost), while higher frequencies will solve the problem. Note that frequencies higher than 450 MHz may produce clock violations. Thus, the typical adjust range goes from 380 to 420 MHz.

[-t] [--freq_steps] The step size of the calibration test in MHz. For low values (< 5 MHz), the optimal frequency can be optimized, but the calibration time will increase dramatically. Moreover, not all the frequencies

can be synthesized due to internal PLL limitations (M/N factor).

[-s] [--events_progress] When the acquisition is set by the number of events, this option lets user to select every how many events the INFO message will appear with the current number of captured events.

Example 1 This example calibrates the all the FPGA-TDC channels with 100000 events generated by an external PPG connected to TDC_CALIB_PULSE SMA port. As for the optimization values, the clearance is set to 3, and the range of internal PLL frequencies to test ranges from 380 to 420 MHz:

hrflextot tdc_calib -e 100000 -o hrft_calib.txt -P -i 3 -r 380 420

History Legacy command.

2.3.6 hrflextot tdc_acq

Command hrflextot tdc_acq <[-e <n_evts>] [-m <n_msecs>]> <-i calib_file> <-o output_file> [-P] [-D bin_dump_file] [-f n_frames] [-M rate_kevts] [-W pwidth_ns] [-p size_bytes] [-E <ch_wildcard>] [-k] [-c] [-s n_events]

Acquires ToT pulses for each of the 16 HR-FlexToT channel outputs and and

[-e] [--events] The number of total events to read before stopping acquisition. One event corresponds to a pulse, where rising edge is the Time-of-Arrival, and the difference between rising and falling edge is the pulse width.

[-m] [--msecs] The acquisition time of the test in milliseconds. Note that either number of events or acquisition time must be provided.

[-i] [--calib_file] The calibration file generated by *tdc_calib* command, which contains a lookup table to convert acquired events into picoseconds units. It is important to highlight that each board has its own calibration file, and this can also vary after a firmware upgrade.

[-o] [--output_file] The name of the CSV file containing the acquired events. The file contains as many rows as events, and each row contains the Event ID, the HR-FlexToT channel number (from 0 to 15), the timestamp (in ps) corresponding to the ToA, and finally the pulse width (in ps). The software automatically fixes the FPGA ToA counter overflow which occurs every ~100 ms. Note that, unless the coarse counter external reset capability is enabled, the first ToA timestamp will be an arbitrary value. A second file with the suffix *.uncalib.txt* is also generated. It contains the TDC information as it arrives from the FPGA. This file is very useful for troubleshooting purposes.

[-P] [--calib_pulse] When this option is provided, all the TDC channels will rely on TDC_CALIB_PULSE SMA input port. This can be very useful to calibrate the board with an external pulse generator.

[-D] [--raw_dump_file] Dumps the data coming from the USB in raw format file. It can be useful to trace and report errors.

[-f] [--frames_between_checks] A checkpoint byte is added every N data frames coming from the USB acquisition system. This byte is useful to check data alignment and to ensure that no data is lost in the transmission. The minimum value is 16 and the maximum is 4080. The default value does not need to be changed.

[-M] [--max_rate_kevts] The maximum acquisition rate can be limited in case that the acquisition system host is not powerful enough (e.g. Raspberry Pi or similar). Apply this filter only if the number of checkpoint issues (use the -l debug option for debugging) grows substantially (hundreds of errors per

second).

[-W] [--min_pwidth] This option prevents the FPGA to send TDC events the pulse of which is lower than a certain value. This is very useful to reduce the capture file size and also to prevent USB DAQ throttling. The value is specified in nanoseconds.

[-p] [--packet_size] Length (in bytes) of the USB packet to be read. Big packet sizes are more efficient in terms of throughput.

[-E] [--en_channels] This option lets the user to individually enable/disable TDC-FPGA channels. When using this option, a list of 16 values with either 0 or 1 value must be provided. Channel 0 corresponds enable corresponds to the first value, while the last value for channel 15. All channels are enabled by default.

[-k] [--clk_mon] When this option is provided, a copy of the TDC-FPGA internal reference clock is output though TDC_CLK_MON_SE SMA output port and TDC_CLK_MON LVDS output port. This is useful to synchronize two boards with the same reference clock.

[-c] [--coarse_rst] When this option is provided, TDC_COARSE_RST SMA port is used to reset the TDC-FPGA global coarse counter. This is useful to synchronize different boards.

[-s] [--events_progress] When the acquisition is set by the number of events, this option lets user to select every how many events the INFO message will appear with the current number of captured events.

Example 1 This example acquires during 5 seconds from the 16 FPGA-TDC channels. The calibration file is *hrft_calib.txt* and the converted events are stored into *tdc_data.txt* file.

hrflextot tdc_acq -s 5000 -i hrft_calib.txt -o tdc_data.txt

History Legacy command.

2.3.7 hrflextot info

Command hrflextot info

Shows HR-FlexToT board useful information. No command options are required.

Example hrflextot info

History Legacy command.

2.3.8 hrflextot config

Command hrflextot config [--auto_reload] [--calib_sel <ch>] [--trg_sel_asic <src>] [--trg_sel_fpga <src>] [--fsm_mon <state>] [--dis_trg_mon] [--vth_pd <vth>] [--vth_eos <vth>] [--vth_soc <vth>] [--vth_eoc <vth>] [--pwidth_rst <width>] [--pwidth_armed <width>] [--pwidth_shaper <width>] [--gain <value>] [--gain_rl <value>] [-f config_file] [-s] [-S] [-c] [-G] [-D delay_ns] [-a v_anode] [-P v_clip] [-L vin_lim] [-p <res> <cap>] [-k] [-T vth] [-R vth] [-U vth] [-t <ch> <vth> [<ch> <vth> …]] [-r <ch> <vth> [<ch> <vth> …]] [-e <ch> <0/1> [<ch> <0/1> …]] [-i <ch> <0/1> [<ch> <0/1> …]] [-O] [-m <ch> <0/1>] [-M ch]

Configures HR-FlexToT electronics. This command is incremental, i.e. the ASIC parameters only change when user provides a new value. Note that the ASIC can also be configured from a previously generated configuration file which contains the values for all the chip registers. This file is in text format and the name of the registers is the same as in the HR-FlexToT datasheet.

[--auto_reload] This option waits indefinitely for changes in the configuration file provided when the chip is configured using a configuration file. This is useful to modify ASIC parameters directly from the configuration file without needing to call every time the software, which will reconfigure the ASIC every time that file is saved.

[--calib_sel] An external calibration pulse from an SMA port (EXT_CALIB_VA_in) is injected to one of the HR-FlexToT inputs (0-15).

[--trg_sel_asic] ASIC trigger selector. 0 = Cluster, 1 = External, 2 = In Stage, 3 = NL ToT. **IMPORTANT:** a known bug in the ASIC FSM makes unpractical to use the trigger without being filtered. To filter the trigger signal, use --trg_sel_fpga option.

[--trg_sel_fpga] FPGA trigger selector. 0 = Cluster, 1 = External, 2 = In Stage, 3 = NL ToT. The FPGA also has available the 4 selectable trigger signals. When this option is used, the FPGA filters (removes any glitch that may occur in the signal) the selected trigger and then it sends it to the ASIC through its external trigger input. Moreover, there is the option to arbitrary delay this signal (-D option).

[--fsm_mon] FSM dedicated monitoring port. The FSM_MON SMA port will output the selected FSM state. Check the datasheet for the available options.

[--dis_trg_mon] Disables trigger monitoring via CLK_MON SMA connector.

[--vth_pd] Peak Detector (PD) threshold voltage configuration (0-511).

[--vth_eos] End of Shaping (EoS) threshold voltage configuration (0-511).

[--vth_soc] Start of Conversion (SoC) threshold voltage configuration (0-511).

[--vth_eoc] End of Conversion (EoC) threshold voltage configuration (0-511).

[--pwidth_rst] Controls the monostable timer which generates the asynchronous FSM's S_RST state. This allows to modify the pulse width of S_RST state (0-15).

[--pwidth_armed] Controls the monostable timer which generates the asynchronous FSM's S_ARMED state. This allows to modify the pulse width of S_ARMED state (0-15).

[--pwidth_shaper] Controls the monostable timer which generates the asynchronous FSM's S_SHAPER_START state. This allows to modify the shaping time of the ASIC (0-15).

[--gain] Current gain applied in the input stage of the energy paths (0-3).

[--gain_rl] Load resistor that converts the amplified current in the input stage into a voltage (0-3).

[-f]
[--config_file] Loads all HR-FlexToT registers from a configuration file (see *show_config* command to generate this file). When *--auto_reload* option is asserted, user can modify the configuration file and new parameters will be sent to the chip each time the file is saved.

[-s]
[--safe_reset] When asserted, the ASIC configuration is read, chip is reset, and finally the configuration is restored with the new parameters. This will move the internal asynchronous FSM to a known state.

[-S] To bypass the internal ASIC asynchronous FSM. When asserted, the FPGA takes control of the

[--fpga_fsm]	conversion and generates the control signals. The ASIC has dedicated IOs for fast signals (Rd/Wr/Dschg), while the rest are sent via SPI at very high speed. This introduces noise and makes this configuration not suitable for SPTR measurements. Use this flag only for energy measurements.
[-c] **[--clk_disable]**	By default, the software waits for pressing [ENTER] to exit, since the clock is disabled after software ends and FPGA FSM will stop working therefore. Leaving the software running is useful for human debugging the signals with an oscilloscope. However, it may be not practical for automating measurements.
[-G] **[--soft_trigg]**	Assert when FPGA External Trigger is controlled by software (fast command).
[-D] **[--trg_delay]**	Delays filtered trigger. Units in nanoseconds.
[-a] **[--v_anode]**	Input channel DC voltage (Vanode[ch]: 0-511). Format: <ch> <value> [<ch> <value> , ...]
[-P] **[--v_clip]**	Minimum DC voltage at the input stage (anode node) to ensure that input current mirror is in saturation (0-511)
[-L] **[--vin_lim]**	When this option is provided, TDC_COARSE_RST SMA port is used to reset the TDC-FPGA global coarse counter. This is useful to synchronize different boards.
[-p] **[--pz_shaper]**	PZ Shaper parameters. Format <ResPZ> (0-63) <CapPZ> (0-15).
[-k] **[--th_mode]**	Sampler analog output selector. Low: peak detector (default). High: track & hold.
[-T] **[--i_thcoarse]**	Global coarse threshold at the current comparator for time signal (0-63).
[-R] **[--i_thtrgcoarse]**	Global coarse threshold at the current comparator for low level trigger (0-63).
[-U] **[--i_thcluster]**	Global threshold at the current comparator for high level (cluster) trigger (0-63).
[-t] **[--i_thch]**	Threshold at the current comparator for the time signal path (IthCh[ch]: 0-63). Format: <ch> <value> [<ch> <value> , ...]
[-r] **[--i_trgthch]**	Threshold at the current comparator for the low level trigger path (ITRGthCh[ch]: 0-63). Format: <ch> <value> [<ch> <value> , ...]
[-e] **[--energy_oen]**	Linear ToT (energy) channel output enable. (0-1). Format: <ch> <value> [<ch> <value> , ...]
[-i] **[--time_oen]**	Non-Linear ToT (time) channel output enable. Format: <ch> <value> [<ch> <value> , ...]
[-O] **[--fastor_dis]**	Disables non-linear ToT LVDS output.
[-m] **[--v_mon]**	Internal analog signal monitor (SMA VMON_SW/PDH_out). Format <ch> (0-15) <shaper=0/peak=1>

[-M] ASIC binary outputs monitor (SMA ENRGY_TIME). Format <ch> (0-15) <shaper=0/peak=1>

[--d_mon]

Example 1 This example loads the ASIC configuration stored into hrft_config.txt file and then waits for changes on that file. Every time the file is saved (modification time changes), the parameters are reloaded into the chip.

hrflextot config --auto_reload -f hrft_config.txt

Example 2 This example configures the external FSM mode, modifies Vanode[4] to 314 LSBs, configures the pole/zero shaper with R=14 and C=12, and changes the coarse trigger threshold to 58.

hrflextot config -S -a 4 314 -p 14 12 -R 58

History Legacy command.

2.3.9 hrflextot show_config

Command hrflextot show_config [-w hex_word] [-o file] [-m] [-D]

Shows HR-FlexToT registers configuration. It also allows to dump this configuration into a file, so that then can be modified or configured to the board.

[-w]
[--spi_loopback_word] The last SPI Slave register address (0xFF) is a loopback, i.e. MOSI is bypassed to MISO, so that the expected read value should be the same as the transmitted value, and thus communication issues can be debugged. With this option, user can choose which loopback 16-bit word (in hexadecimal format) is going to be transmitted. For debugging purposes only.

[-o]
[--dump_config_file] Dump current configuration to the specified file.

[-m]
[--map] Gets the SPI bit map of the ASIC registers. For debugging purposes only.

[-D]
[--dec] Shows register values in decimal format (hexadecimal by default).

Example This example shows the current ASIC configuration in decimal format and stores them into my_hrft_conf.txt:

hrflextot show_config -D -o my_hrft_conf.txt

History Legacy command.

2.3.10 hrflextot threshold_scan

Command hrflextot threshold_scan <-r out_file> [-w window_us] [-T vth] [-s step] [-R vth] [-S step] [-c LSBs] [-e <ch> <0/1> [<ch> <0/1> …]]

Runs a threshold scan of all the binary discriminated outputs on the chip: time (16), low-level trigger (16) and high-level trigger (1). It performs a sweep of the comparator V_{TH} to find the value where the output channel transition.

[-r] Specify the results file name. Mandatory.

[--results]

[-w] Select the duty cycle analysis window (in us). For each threshold scan step, a time window of this size is taken and duty cycle is measured. The maximum number must not exceed 166000 us (10000 us by default). The higher the number, the better measurement accuracy, but test time dramatically increases.

[--dutywindow]

[-R] Select the first trigger coarse threshold to scan (0 < IbTRGthCoarse < 63).

[--min_trgthcoarse]

[-s] Select timing coarse threshold step width.

[--step_thcoarse]

[-R] Select the first trigger coarse threshold to scan (0 < IbTRGthCoarse < 63).

[--min_trgthcoarse]

[-S] Select trigger coarse threshold step width.

[--step_thtrgcoarse]

[-c] Time discriminator clearance (in LSBs) wrt IthCh[ch] which produces the discriminator transition from 0 to 1. Once threshold scan ends, the software prints the optimal configuration to be configured. If this parameter is not provided, the list of values will be the ones where the transitions occur. On the contrary, if this parameter is passed, the list of values displayed will be N LSBs from the transition.

[--clearance]

[-e] Channel enable for this test (0-1). Format: <ch> <value> [<ch> <value> , ...].

[--ch_enable]

Example This example performs a threshold scan with 40 us duty cycle window, stores the results into hrft_th_scan.txt file, and show the optimal threshold configuration thresholds at 8 LSBs away from the switching threshold:

```
hrflextot threshold_scan -c 8 -w 40000 -r hrft_th_scan.txt
```

History Legacy command.

2.3.11 hrflextot photon_count

Command hrflextot photon_count [-m ms] <-r outfile> [-v <min> <max>] [-V <min> <max>] [-e <ch> <0/1> [<ch> <0/1> …]]

Performs a photon count rate test. When no V_{TH} range is specified, the measurement will correspond to the number of binary pulses occurred in Fast-OR timing output (TIME_SE_out SMA). When a range is provided, the dark staircase function is obtained.

[-m] Select the capture time (in milliseconds) for the photon count measurement (100 ms default). The higher the value, the better accuracy and the higher test time.

[--milliseconds]

[-r] Specify the results file name. Mandatory.

[--results]

[-v] Select the range (<min> <max>) of channel timing comparator V_{TH} to perform the photon count rate V_{TH} sweep. When the option is not specified, the test is performed only once with the current

[--vth_range]

chip V_{TH} configuration. (0 < ICTth[ch] < 63).

[-V] [--coarse_range] Select the range (<min> <max> <step>) of coarse timing comparator V_{TH} to perform the photon count rate V_{TH} sweep. When no specified, the test is performed once with the current chip coarse V_{TH} configuration. (0 < IbITthCoarse < 63).

Example This example performs a photon count rate test where the capture time per step is 200 ms, and the results file is hrft_dcr.txt.

hrflextot photon_count -m 200 -r hrft_dcr.txt

History Legacy command.

2.4 Example of HR-FlexToT usage using an electrical signal

The following example shows the signal outputs when an electrical signal is injected into the ASIC. The following test requires the following instrumentation.

1. Arbitrary Waveform Generator.
2. Low voltage power supply.
3. Personal Computer
4. Attenuators

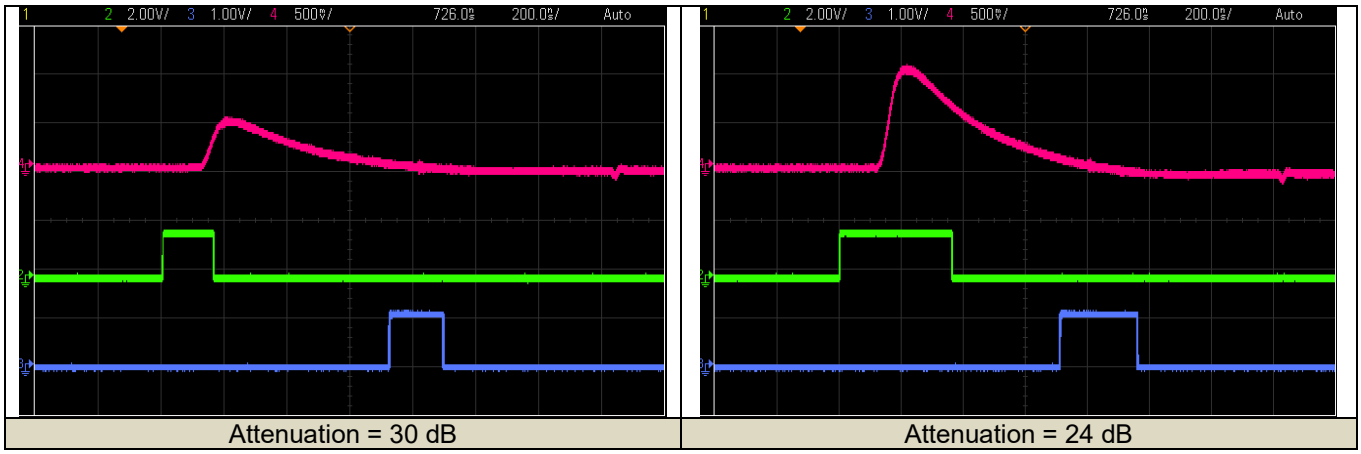
Do the following steps to reproduce the test, please.

1. Generate a SiPM-like pulse shape of 4 Vpp. The input is AC coupled, so do not worry about the offset. A pulse rate of 10 KHz is ok (despite it can hande > 1 MHz with the internal ASIC FSM).
2. Connect the output to a programmable attenuator.
3. Connect the attenuator output to EXT_CALIB_VA_in SMA input of the HR-FlexToT board.
4. Connect the following SMA outputs to an oscilloscope:
   - VMON_SW/PDH_out: purple plot.
   - TIME_SE_out: green plot.
   - ENERGY_TIME: blue plot.
5. Run the following command with the HRFlexToT software:

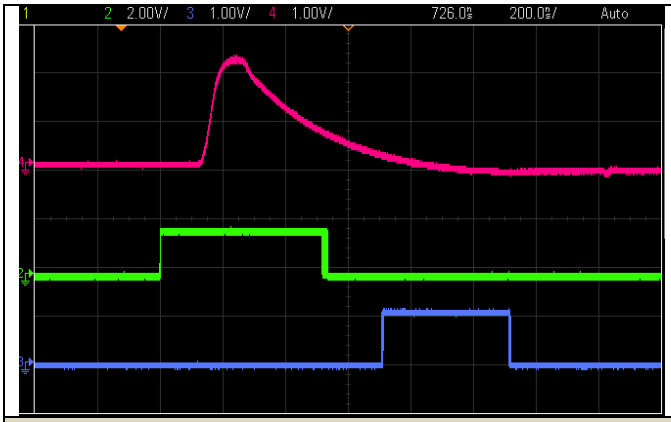
```
$ sw/hrflextot config -s -S --gain 3 --gain_rl 3 -R 61 -T 55 -k 0
-r 0 20 --calib_sel 0 -m 0 0 -M 0

20180730T112946 I Trigger Settings:
20180730T112946 I    - External (FPGA): Input Stage (LLT)
20180730T112946 I    - Trigger monitoring (SMA U4): Enable
20180730T112946 I
20180730T112946 I FPGA system settings:
20180730T112946 I    - Compatibility MUX: 1
20180730T112946 I
20180730T112946 I User-defined FPGA settings:
20180730T112946 I    - ASIC FSM controlled by the FPGA
20180730T112946 I
20180730T112946 I User-defined ASIC global settings:
20180730T112946 I    - THMode = 0
```

```
20180730T112946 I    - G = 3
20180730T112946 I    - RL = 3
20180730T112946 I    - IbIIthCoarse = 55
20180730T112946 I    - IbTRGthCoarse = 61
20180730T112946 I    - TrgSel = 1
20180730T112946 I    - CalibChSel = 0
20180730T112946 I    - MonPnS = 0
20180730T112946 I    - MonChSel = 0
20180730T112946 I    - Digital Monitoring: ON
20180730T112946 I      - ASIC Output CH[0]
20180730T112946 I    - FSM Debug Mode: OFF (!FPRBE = 1)
20180730T112946 I
20180730T112946 I User-defined ASIC channel settings:
20180730T112946 I    - ITRGthCh[0] = 20
20180730T112946 I
20180730T112946 I Channel output configuration:
20180730T112946 I    - CH[ 0]: ON  ( - , E )
20180730T112946 I    - CH[ 1]: ON  ( - , E )
20180730T112946 I    - CH[ 2]: ON  ( - , E )
20180730T112946 I    - CH[ 3]: ON  ( - , E )
20180730T112946 I    - CH[ 4]: ON  ( - , E )
20180730T112946 I    - CH[ 5]: ON  ( - , E )
20180730T112946 I    - CH[ 6]: ON  ( - , E )
20180730T112946 I    - CH[ 7]: ON  ( - , E )
20180730T112946 I    - CH[ 8]: ON  ( - , E )
20180730T112946 I    - CH[ 9]: ON  ( - , E )
20180730T112946 I    - CH[10]: ON  ( - , E )
20180730T112946 I    - CH[11]: ON  ( - , E )
20180730T112946 I    - CH[12]: ON  ( - , E )
20180730T112946 I    - CH[13]: ON  ( - , E )
20180730T112946 I    - CH[14]: ON  ( - , E )
20180730T112946 I    - CH[15]: ON  ( - , E )
20180730T112946 I
20180730T112946 I Press [ENTER] to exit…
```

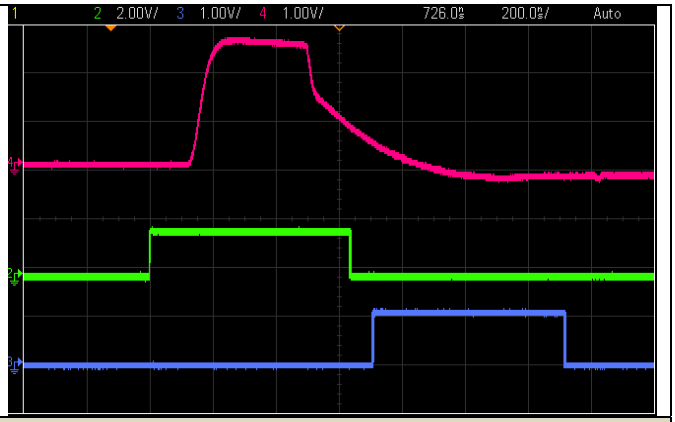
6. Decrease attenuation in 6-dB steps.
7. Additionally, Energy signal ToT can be measured by means of the built-in FPGA-TDC.



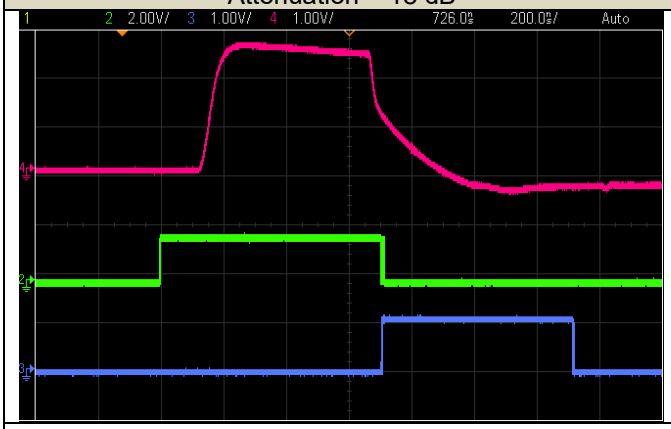
Attenuation = 30 dB | Attenuation = 24 dB



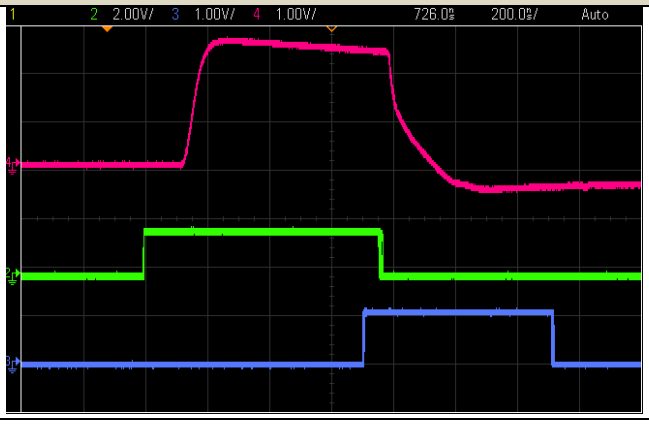
Attenuation = 18 dB



Attenuation = 12 dB



Attenuation = 6 dB



Attenuation = 0 dB